## Intel in HPC -Intel Software Development Tools

eXtreme XQCD Bern \_Aug 5<sup>th</sup>, 2013 Edmund Preiss Manager Business Development, EMEA

# **Topics Covered Today**

- Intel's offerings to HPC
- Update on Intel Architecture Roadmap
- Overview on Intel Development Tools for (hybrid) HPC and SMP Systems
- Intel Development Support for Intel Xeon Processors and Intel Xeon Phi Coprocessor
  - Considerations of Porting existing X86 Applications
  - Programming Models
  - How to start with MIC Architecture
- More Details and Benefits of Intel Development Tools





## Intel in HPC

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### The Three Pillars of Modern Science, Research & Engineering







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## Efficiency at Scale in Supercomputing

### **Top500\*** (1997 – 2012)



Driven by Moore's Law and Architecture Innovation



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### **Intel Road Map and Architectures**





Intel® Xeon Phi<sup>™</sup> Coprocessor extends established CPU architecture and programming concepts to highly parallel applications

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### Next Intel<sup>®</sup> Xeon Phi<sup>™</sup>Processor: Knights Landing



Designed using Intel's cutting-edge 14nm process

Not bound by "offloading" bottlenecks **Standalone CPU or PCIe Coprocessor** 

Leadership compute & memory bandwidth Integrated On-Package Memory

All products, computer systems, dates and figures specified are preliminary based on current expectations, and are subject to change without notice.



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### Intro to Intel Software Dev Tools & Usefulness for Intel Xeon and Intel Xeon Phi







Phase	Product	Feature	Benefit
	Intel <sup>®</sup> Advisor XE	Threading design assistant (Studio products only)	<ul> <li>Simplifies, demystifies, and speeds parallel application design</li> </ul>
Build	Intel® Composer XE	<ul> <li>C/C++ and Fortran compilers</li> <li>Intel® Threading Building Blocks</li> <li>Intel® Cilk™ Plus</li> <li>Intel® Integrated Performance Primitives</li> <li>Intel® Math Kernel Library</li> </ul>	<ul> <li>Enabling solution to achieve the application performance and scalability benefits of multicore and forward scale to many-core</li> </ul>
	Intel <sup>®</sup> MPI Library <sup>†</sup>	High Performance Message Passing (MPI) Library	<ul> <li>Enabling High Performance Scalability, Interconnect Independence, Runtime Fabric Selection, and Application Tuning Capability</li> </ul>
	Intel <sup>®</sup> VTune™ Amplifier XE	Performance Profiler for optimizing application performance and scalability	<ul> <li>Remove guesswork, saves time, makes it easier to find performance and scalability bottlenecks</li> </ul>
Verify & Tune	Intel <sup>®</sup> Inspector XE	Memory & threading dynamic analysis for code quality Static Analysis for code quality	<ul> <li>Increased productivity, code quality, and lowers cost, finds memory, threading, and security defects before they happen</li> </ul>
	Intel <sup>®</sup> Trace Analyzer & Collector	MPI Performance Profiler for understanding application correctness & behavior	<ul> <li>Analyze performance of MPI programs and visualize parallel application behavior and communications patterns to identify hotspots</li> </ul>



### **Highly Parallel Applications**



Theoretical acceleration of a highly parallel processor over a Intel® Xeon® parallel processor (<1: Intel® Xeon® faster) – For illustration only

Efficient vectorization, threading, and parallel execution drives higher performance for suitable applications

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### How to get Started with Xeon Phi

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INTEL HPC		Get Started	23
V	www.intel.com/xeonphi	Download the programming guide to find out whether your workload can benefit from Intel® Xeon Phi™ coprocessors:	
	(intel)	software.intel.com/mic-developer	
	inside <sup>™</sup> XEON PHI <sup>™</sup>	Link to Best Practices (for Xeon Phi)	
		<u>http://www.prace-ri.eu/IMG/pdf/Best-Practice-</u> <u>Guide-Intel-Xeon-Phi.pdf</u>	



### http://software.intel.com/mic-developer

Intel® Xeon Phi™ Coprocessor (codename Knights Corner)

http://software.intel.com/en-us/articles/intel-xeon-phi-coprocessor-codename-knights-corner

Intel® Xeon Phi<sup>™</sup> Coprocessor Instruction Set Architecture Reference Manual http://software.intel.com/en-us/articles/optimization-and-performance-tuning-for-intel-xeon-phi-coprocessors-part-2-understanding

An Overview of Programming for Intel® Xeon® processors and Intel® Xeon Phi<sup>™</sup> coprocessors http://software.intel.com/sites/default/files/article/330164/an-overview-of-programming-for-intel-xeon-processors-and-intel-xeon-phi-coprocessors\_1.pdf

Intel® Manycore Platform Software Stack (MPSS) http://software.intel.com/en-us/articles/intel-manycore-platform-software-stack-mpss

Intel® Xeon Phi<sup>™</sup> Coprocessor Developer's Quick Start Guide http://software.intel.com/en-us/articles/intel-xeon-phi-coprocessor-developers-quick-start-guide

Programming and Compiling for Intel® Many Integrated Core Architecture http://software.intel.com/en-us/articles/programming-and-compiling-for-intel-many-integrated-core-architecture

Intel® Xeon Phi™ Coprocessor System Software Developers Guide http://software.intel.com/sites/default/files/article/334766/intel-xeon-phi-systemsoftwaredevelopersguide.pdf

Intel and Third Party Tools and Libraries available with support for Intel® Xeon Phi™ Coprocessor http://software.intel.com/en-us/articles/intel-and-third-party-tools-and-libraries-available-with-support-for-intelr-xeon-phitm

Optimization and Performance Tuning for Intel® Xeon Phi™ Coprocessors - Part 1: Optimization Essentials http://software.intel.com/en-us/articles/optimization-and-performance-tuning-for-intel-xeon-phi-coprocessors-part-1-optimization

Optimization and Performance Tuning for Intel® Xeon Phi<sup>™</sup> Coprocessors, Part 2: Understanding and Using Hardware Events http://software.intel.com/en-us/articles/optimization-and-performance-tuning-for-intel-xeon-phi-coprocessors-part-2-understanding

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### **Books for Parallelisation and Xeon Phi Programming**



#### Structured Parallel Programming

Michael McCool, Arch D. Robinson, and James Reinders, ISBN 978-0-124-15993-8 (Morgan Kaufmann)

Intel<sup>®</sup> Xeon Phi<sup>™</sup> Coprocessor High Performance Programming



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#### Intel Xeon Phi Coprocessor High Performance Programming

Jim Jeffers and James Reinders (Morgan Kaufmann) Publication Date: March 1, 2013 | ISBN-10: 0124104142 | ISBN-13: 978-0124104143 | Edition: 1



### **Books for Parallelisation and Xeon Phi Programming**





Parallel Programming with Intel® Parallel Studio XE treat a Jacobio Nuclear Charge Ju., Andrew Stokes

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Parallel Programming and Optimization with Intel<sup>®</sup> Xeon Phi<sup>™</sup> Coprocessors [517 Pages]

Handbook on the Development and Optimization of Parallel Applications for Intel<sup>®</sup> Xeon<sup>®</sup> Processors and Intel<sup>®</sup> Xeon Phi<sup>™</sup> Coprocessors

ISBN 9780988523418

www.colfax-intl.com/xeonphi/book.html

#### Parallel Programming with Intel Parallel Studio XE

Handbook on the Development and Optimization of Parallel Applications for Intel X86 CPUs using Shared Memory Programming Models (Textbook for Intel Parallel Studio XE)

2012, publisher: Worx



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### http://software.intel.com/mic-developer

### Highly recommended reading:

An Overview of Programming for Intel® Xeon® processors and Intel® Xeon Phi<sup>TM</sup> coprocessors Submitted by James Reinders ... on Mon, 11/12/2012 - 12:59



## **Key Elements of Intel Tools Functionality**

Performance Optimisation

Parallelisation

Correctness of Applications



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Fortran	Compile	er Compa	rison — Ir	ntel CPU	(3 <sup>rd</sup> part	<b>y</b> )				
ortran Execution Time Benchmarks - 64-bit Scientific Linux on Intel Core i5 2500k										
	Absoft 11.1.3	<b>G95</b> 0.93	GFortran 4.7.2	<i>Intel</i> 13.0	Lahey 8.10b	<b>PGI</b> 12.9	<b>Sun</b> 8.6			
AC	4.41	9.60	5.92	4.94	8.00	7.13	21.99			
AERMOD	11.95	25.99	18.99	10.53	11.27	11.91	10.30			
AIR	3.46	5.95	3.10	2.34	2.71	3.85	2.51			
CAPACITA	18.38	26.83	17.96	16.83	19.94	16.98	21.56			
CHANNEL2	102.78	272.72	84.26	85.39	122.19	105.71	84.83			
DODUC	17.24	24.05	17.51	14.10	17.45	17.30	14.15			
FATIGUE2	68.78	374.38	101.73	72.12	110.88	87.30	75.28			
GAS_DYN2	84.14	320.04	86.71	69.01	107.03	66.20	84.39			
INDUCT2	73.67	147.53	66.57	67.00	93.29	118.24	125.91			
LINPK	5.57	6.21	5.77	4.88	5.67	5.37	5.11			
MDBX	8.68	8.68	7.32	6.03	7.85	8.35	7.41			
MP_PROP_DESIGN	74.41	419.95	103.67	60.22	126.05	86.13	161.97			
NF	7.69	13.40	7.79	7.30	10.36	7.71	8.16			
PROTEIN	19.88	27.43	20.33	18.12	35.68	20.75	20.44			
RNFLOW	13.77	25.90	15.47	11.67	14.58	16.66	15.72			
TEST_FPU2	72.11	103.38	42.94	43.73	61.17	42.77	57.41			
TFFT2	55.10	60.04	54.16	53.49	55.74	55.38	55.07			
Geometric Mean	22.18	43.13	22.94	18.95	26.07	23.25	25.04			
			• • • •							
		Source:	http://www.	polyhedron.c	om		(i=1=1			
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	intelº Cilk™ Plus	Intel <sup>®</sup> Threading	Domain-Specific	Established	Research and				
		Building Blocks	Libraries	Standards	Development				
	C/C++ language extensions to simplify parallelism	Widely used C++ template library for parallelism	Intel <sup>®</sup> Integrated Performance Primitives	Message Passing Interface (MPI)	Intel <sup>®</sup> Concurrent Collections				
			Intel <sup>®</sup> Math Kernel	OpenMP*	Offload Extensions				
			Library	Coarray Fortran	Intel <sup>®</sup> SPMD Parallel Compiler				
	Open sourced &	Open sourced &		OpenCL*					
	Also an Intel product	Also an Intel product							
	Ch	oice of high-perfo	ormance parallel p	programming mod	els				
	Applic	cable to Multico	ore and Many-o	core Programm	ing *				
* Integra	* Integrated Performance Primitives not available for Intel MIC Architecture								



### Scale Performance

### **Tune Hybrid Cluster MPI and Thread Performance**

#### Intel® Trace Analyzer and Collector



#### **Tune cross-node MPI**

- Visualize MPI behavior
- Evaluate MPI load balancing
- Find communication hotspots



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	[DINPUT8.dll]	19.359s			13	0.002s	Constant	
	BaseThreadInitTI	hunk < 19.359s			13	0.002s	Constant	
	timeEndPeriod	19.173s			1,974	0s	Constant	
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								-
	N. CH	and the frame				- L	C	_

### Tune single node threading

- Visualize thread behavior
- Evaluate thread load balancing
- Find thread sync. bottlenecks



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### Dynamic Analysis Finds Memory & Threading Errors Intel<sup>®</sup> Inspector XE 2013



#### Find and eliminate errors

- Memory leaks, invalid access...
- Races & deadlocks
- Analyze hybrid MPI cluster apps
- Heap growth analysis

#### • Faster & Easier to use

- Debugger breakpoints
  - Break on selected errors
  - Run faster to known error
- Pause/resume collection
  - Narrow analysis focus
  - Better performance
  - Improved error suppression

	De	Detect Deadlocks and Data Races				Intel Inspe	ctor XE 20	13		
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Pro	blem	5								8
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Des	criptio	n	Source	Fur	nction	Modu	le			-
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	268	{						find_and_fix_t	hreading_er	
	269		if(!run	ning) re	eturn	false;		find_and_fix_t	hreading_er	
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	272		eise if	(g_nand.	Les[1]	) {				-

#### Find Errors Early When They are Less Expensive

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### Static Analysis Finds Coding and Security Errors



Intel Inspector XE 2013

### • Find over 250 error types e.g.:

- Incorrect directives
- Security errors
- Easier to use  $\bullet$

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- Choose your priority: •
  - Minimize false errors
  - Maximize error detection

## Increased Accuracy & Speed Detect errors without all source files

- Better scaling with large code bases ٠

### **Code Complexity Metrics**

Find code likely to be less reliable

#### Summary ID **9** Problem Sources State Wei. - Category A Ne find and fix nd\_and\_fix\_memory\_errors.cpp(175): error #12375: referenced memory allocated at (file:find\_and\_fix\_memory\_errors.cpp line:170) through "operator new" is illegally deallocated through "free P2 🙆 Divide by zero (possible) cylinder.cpp 🛛 P Confirm... 75 Other cylinder.cpp(131): error #12062: possible divide by zero P7 🙆 Unsafe format specifier parse.cpp 🖌 🖌 Fixed 70 Format parse.cpp(187): error #12329: specify field width in format specifier to avoid buffer overflow on argument 3 in call to "fscanf Code Locations: Bad free Description Source Function Variable Deallocation site find\_and\_fix\_memory\_errors.... void draw\_task::operator()(cl ... 173 drawing->put pi void draw task::operator() 174 175 free(drawing); // 176 //delete drawing; 177 Allocation site find\_and\_fix\_memory\_errors.... void draw\_task::operator()(cl ... 168 for (int y = r.begin(); y ! void draw\_task::operator() 169 170 171 172 drawing area \* draw for (int x = startx color t. c = ret

Static Security Analysis Result

### Find Errors and Harden your Security

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## **Conditional Numerical Reproducibility**



- Intel<sup>®</sup> Math Kernel Library:
  - New deterministic task scheduling and code path selection options
- OpenMP:
  - New deterministic reduction option
- Intel<sup>®</sup> Threading Building Blocks
  - New parallel deterministic reduce option

### Help Achieve Reproducible Results, Despite Non-associative Floating Point Math

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# Win a Lenovo Notebook

- Come to our stand and fill in Raffle card
- Join the Raffle Drawing
  - Tuesday 6<sup>th</sup> August
  - 3:45 PM
  - @ Intel Stand
- You need to be present at Drawing in order to win



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